What is claimed is:

1. A semiconductor integrated circuit device having a plurality of internal circuits operable in synchronism with an internal clock, comprising:

a clock generating circuit for generating a first clock having a predetermined period;

an intermittent clock generating circuit for generating a second clock which comprises an intermittent train of pulses produced by removing some pulses from said first clock, and supplying said second clock as said internal clock to said internal circuits; and

a current generating circuit for consuming a power supply current in timed relation to a third clock which comprises a train of pulses to be removed from said first clock.

2. The semiconductor integrated circuit device according to claim 1, wherein said intermittent clock generating circuit comprises:

a variable data output circuit for outputting data which is variable with time;

a timing generator for generating said third clock according to the data output from said variable data output circuit; and

a synchronizing circuit for generating said second clock by being supplied with said third clock and said first clock output from said clock generating circuit and stopping outputting said first clock in timed relation to said third clock.

3. The semiconductor integrated circuit device according to claim 2, wherein said variable data output circuit is a random number generator for

generating a random number.

4. The semiconductor integrated circuit device according to claim 1, further comprising:

a current generating circuit group comprising a plurality of said current generating circuits; and

a circuit selecting register for selecting at least one of said current generating circuits which is to consume said power supply current, according to a prestored value.

5. The semiconductor integrated circuit device according to claim 2, further comprising:

a current generating circuit group comprising a plurality of said current generating circuits; and

a circuit selecting register for selecting at least one of said current generating circuits which is to consume said power supply current, according to the data output from said variable data output circuit.